Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. **(Currently Amended)** A method for the compensation of interference in a signal generated by discrete multitone modulation, the interference essentially being caused by the transient process of a transmission channel via which the signal is transmitted, the signal having a multiplicity of symbols with digitized samples and each symbol being preceded by a cyclic prefix with digitized samples, the method having the following steps:

feeding of the digitized samples of the signal to a serial/parallel converter (15);

calculation of a difference between ~~subtraction of~~ at least one digitized sample of a symbol [[from]] and a digitized sample ~~assigned thereto~~ of the cyclic prefix preceding the symbol by means of at least one subtractor circuit (16), ~~for~~ thereby determining interference;

calculation of the transient process of the transmission channel from the determined interference by means of multiplier circuits (17, 18); and

calculation of a difference between ~~subtraction of~~ the calculated transient process [[from]] and the digitized samples of the symbol.

2. **(Currently Amended)** The method as claimed in claim **1**, characterized in that provision is made of corresponding devices (4, 8; 5, 10; 7, 12) for compensation of the interference ~~both~~ in the time domain ~~and in the frequency domain~~.

3. **(Currently Amended)** The method as claimed in claim **1**, characterized in that coefficients which are calculated from [[the]] an error-corrected digitized samples are fed to a system analysis unit (6) from which the properties of the transmission channel are calculated.

4. **(Currently Amended)** A circuit arrangement for carrying out the method as claimed in claim **1**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal are providable ~~can be fed~~;

at least one subtractor circuit (16), each subtractor circuit (16) calculating a difference between ~~subtracting~~ a digitized sample of the symbol [[from]] and a digitized sample assigned thereto of the cyclic prefix preceding the symbol for a calculation of [[the]] an error on account of the transient process; and

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, the at least one multiplier circuit (17, 18) being assigned to each digitized sample of [[a]] the symbol;

~~it being possible for~~ wherein the output signal of each subtractor circuit (16) ~~to be fed~~ is providable in each case to each multiplier circuit (17, 18); and

~~it being possible for~~ wherein the output signal of each multiplier circuit (17, 18) ~~to be subtracted~~ is subtractable from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

5. (Currently Amended) The method as claimed in claim **2**, characterized in that coefficients [[which]] that are calculated from [[the]] an error-corrected digitized samples are fed to a system analysis unit (6) from which the properties of the transmission channel are calculated.

6. (Currently Amended) A circuit arrangement for carrying out the method as claimed in claim **2**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal are providable ~~can be fed~~;

at least one subtractor circuit (16), each subtractor circuit (16) calculating a difference between ~~subtracting~~ a digitized sample of the symbol [[from]] and a digitized sample assigned thereto of the cyclic prefix preceding the symbol for a calculation of [[the]] an error on account of the transient process; and

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, the at least one multiplier circuit (17, 18) being assigned to each digitized sample of [[a]] the symbol;

~~it being possible for~~ wherein the output signal of each subtractor circuit (16) ~~to be fed~~ is providable in each case to each multiplier circuit (17, 18); and

~~it being possible for~~ wherein the output signal of each multiplier circuit (17, 18) ~~to be subtracted~~ is subtractable from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

7. **(Currently Amended)** A circuit arrangement for carrying out the method as claimed in claim **3**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal are providable ~~can be fed~~;

at least one subtractor circuit (16), each subtractor circuit (16) calculating a difference between ~~subtracting~~ a digitized sample of the symbol [[from]] and a digitized sample assigned thereto of the cyclic prefix preceding the symbol for a calculation of [[the]] an error on account of the transient process; and

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, the at least one multiplier circuit (17, 18) being assigned to each digitized sample of [[a]] the symbol;

~~it being possible for~~ wherein for the output signal of each subtractor circuit (16) ~~to be fed~~ is providable in each case to each multiplier circuit (17, 18); and

~~it being possible for~~ wherein the output signal of each multiplier circuit (17, 18) ~~to be subtracted~~ is subtractable from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

8. **(Currently Amended)** A circuit arrangement for carrying out the method as claimed in claim **5**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal are providable ~~can be fed~~;

at least one subtractor circuit (16), each subtractor circuit (16) calculating a difference between ~~subtracting~~ a digitized sample of the symbol [[from]] and a digitized sample assigned thereto of the cyclic prefix preceding the symbol for a calculation of [[the]] an error on account of the transient process; and

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, the at least one multiplier circuit (17, 18) being assigned to each digitized sample of [[a]] the symbol;

~~it being possible for~~ wherein the output signal of each subtractor circuit (16) ~~to be fed~~ is providable in each case to each multiplier circuit (17, 18); and

~~it being possible for~~ wherein the output signal of each multiplier circuit (17, 18) ~~to be subtracted~~ is subtractable from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

9. **(New)** The method as claimed in claim 1, characterized in that provision is made of corresponding devices (4, 8; 5, 10; 7, 12) for compensation of the interference in the frequency domain.

10. **(New)** The method as claimed in claim **9**, characterized in that coefficients which are calculated from the error-corrected digitized samples are fed to a system analysis unit (6) from which the properties of the transmission channel are calculated.

11. **(New)** A circuit arrangement for carrying out the method as claimed in claim **9**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal are providable;

at least one subtractor circuit (16), each subtractor circuit (16) calculating a difference between a digitized sample of the symbol and a digitized sample assigned thereto of the cyclic prefix preceding the symbol for a calculation of an error on account of the transient process; and

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, the at least one multiplier circuit (17, 18) being assigned to each digitized sample of the symbol;

wherein the output signal of each subtractor circuit (16) is providable in each case to each multiplier circuit (17, 18); and

wherein the output signal of each multiplier circuit (17, 18) is from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

12. **(New)** A circuit arrangement for carrying out the method as claimed in claim **10**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal are providable;

at least one subtractor circuit (16), each subtractor circuit (16) calculating a difference between digitized sample of the symbol and a digitized sample assigned thereto of the cyclic prefix preceding the symbol for a calculation of the error on account of the transient process; and

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, the at least one multiplier circuit (17, 18) being assigned to each digitized sample of the symbol;

wherein the output signal of each subtractor circuit (16) is providable in each case to each multiplier circuit (17, 18); and

wherein the output signal of each multiplier circuit (17, 18) is subtractable from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).